EFFECT OF SYSTEM ACTIVITY ON CHIP RELIABILITY

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Abstract

This paper presents the results of an investigation of the effects of system activity on chip reliability. Thermal measurements were taken from die surfaces which were exercised at varying rates and with different types of activity. The results showed significant temperature variations with increased activity. The investigation finds that the activity rate and type of activity can cause thermal degradation and thus decrease the mean time to failure of a chip.

1. Introduction

This investigation was motivated by previous research which showed that system reliability is a dynamic function of the workload. [Iyer 82a, b] and [Castillo 81] provide statistical evidence to support this assertion. Importantly, these studies exhibit the existence of a threshold beyond which an increase in workload resulted in a non-linear increase in the failure rate. One possible reason for the workload/failure dependency is the discovery of latent errors. The issue of error latency in medium and large systems has been studied in [Chillarege 85].

A second possibility is wear out caused by the increased stress resulting from high voltages and currents. In [Cortes 84] this question was examined and an analytical model was proposed to relate device activity and wear out. An important, and as yet unanswered, question is will a higher level of system activity result in significant degradation in the reliability of computer logic devices? Clearly this question has direct relevance to the design of reliable VLSI systems. It was the objective of this investigation to verify experimentally, through infrared scanning, the relationship between system activity and wear out resulting from thermal degradation. In addition we wished to discriminate between various types of system activity as they effect thermal degradation.

2. The Experiment Definition

The aim of the experiment was to determine whether an increase in system activity results in a measurable increase in the surface temperature of a chip. It is well known [Arsenault 80] that temperature accelerates many semiconductor device failure mechanisms. The relationship between the temperature rise and reliability degradation is determined by the Arrhenius plot. Commonly this translates into a temperature related *acceleration factor F.*[1]

$$F \equiv \frac{MTF(T_1)}{MTF(T_2)} \qquad (1)$$

[1]The semiconductor industry, in gathering failure rate data, subjects devices to high temperatures to induce accelerated life conditions.

The *acceleration factor* can be computed as:

$$F = exp\,[\,\frac{E_a}{k}(\frac{1}{T_1} - \frac{1}{T_2})] \qquad (2)$$

where

MTF = Mean Time to Failure

E_a = Thermal Activation Energy[2]

T_1 = Normal Operating Temperature

T_2 = Accelerated Temperature

We measured system activity in two ways; the frequency of an activity and the complexity of the activity. Two types of experiments were performed. The first involved observing the surface temperature of a memory chip while varying the access frequency. The aim was to determine if the access frequency alone could be identified as a variable governing the surface temperature of a chip. A second experiment was set up to observe the temperature of a microcontroller for different levels of complex activity. We defined a base activity as the minimal gate activity (clocking, instruction fetch and decoding) and modeled this by a NOP instruction. At the other extreme, a complex activity was designed to involve the operation of a majority of the functional units of the chip in the data stream. Thus, to model a complex activity we repeated a microcode routine which involved an ALU operation on operands that were fetched indirectly. It was envisioned that such activity would result in a large number of gates changing state. With these higher rates of gate exercise more switching induced transients are likely to be produced in the device. One manifestation of these transients is an increase in temperature at the chip level. The instrumentation

[2]The thermal activation energy of the failure mechanism defines the slope of of the Arrhenius plot which plots accelerated temperature vs accelerated life hours.

for measuring the temperature rise on the chip surface is discussed in the next section.

3. Instrumentation

The experiment employed infrared scanning to measure thermal activity. The device used was an Inframetric 525 IR Scanner [Inframetrics 84]. The scanner is capable of thermal resolution of 0.1 °C and is equipped with a monitor and video camera which allows detailed analysis of the results. The base level is set to the ambient temperature and this is related to a brightness level on the monitor. The relative temperature rise is displayed as the brightening of the area on the monitor. The range of temperature/brightness being viewed is displayed on a monitor scale. The experiment set-up is shown in figure 1. In our experiments the rise above ambient was measured as a function of time. The selection of chips used was qualified by their ease of decapsulation. Measurements were taken from the exposed die.

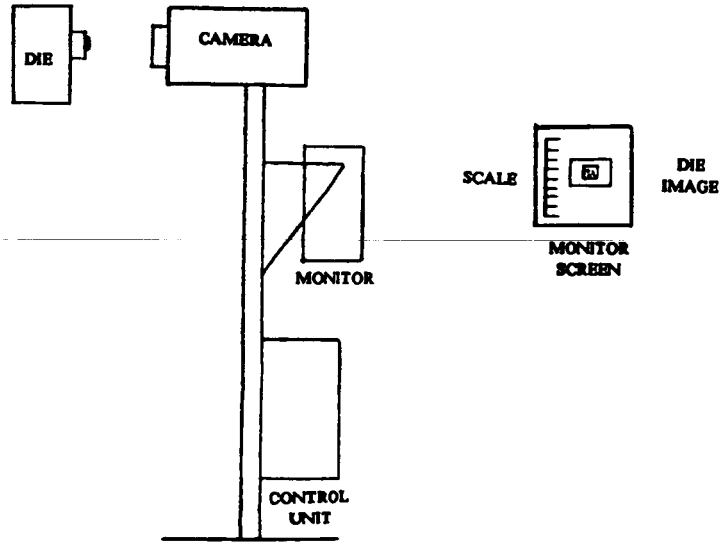

Figure 1: Experiment Setup

4. Memory Chip Measurement

The memory chip used was an Intel 2716 EPROM. The die was observed for read accesses at two rates, 90 KHz and 180 KHz. The experiment showed that the rate at which a chip is accessed can have a significant effect on the temperature increase of the die. The effect of doubling the read access rate is shown in figure 2.

Note that the same access pattern was followed in the experiments isolating frequency of access as the only variable. Thus the result indicates that the memory access circuitry contributes significantly to the temperature rise of the die. The maximum difference is approximately two degrees and there is a pronounced difference in the rate of increase in temperature. The effect of this rise in temperature on reliability depends on the thermal activation energy of the various failure mechanisms involved. The acceleration in failure rate was were computed by equation 2. It is evident from the results that an increase in memory access rate results in reliability degradation. The degradation can vary from 7 to nearly 40 percent depending on the failure mechanism in question (see table 1). Further, the experiment also shows that the access rate of the memory, independent of the combination of logic levels changing states, can be isolated as a variable

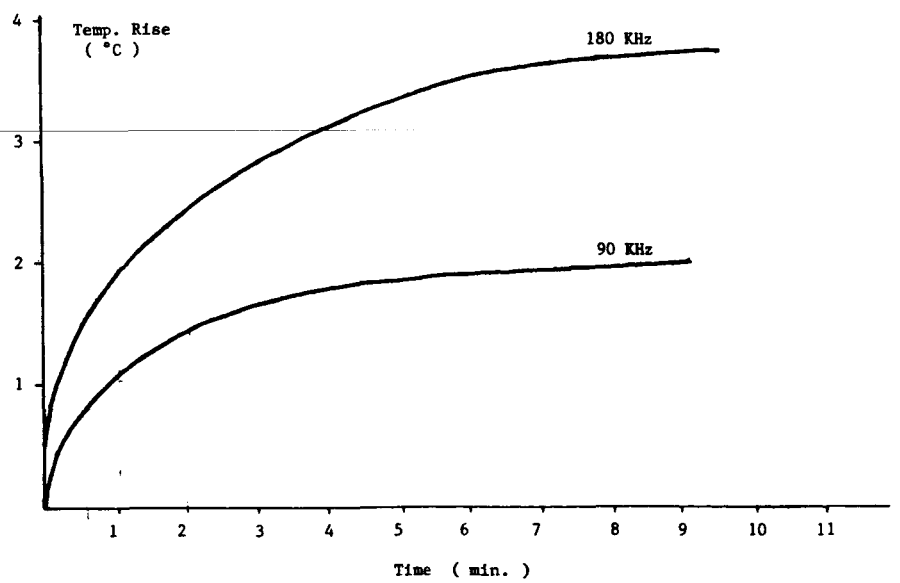

Figure 2: Memory Access Rate Results

controlling reliability degradation.

Memory Read		
Failure Mechanism	Activation Energy	Acceleration Factor
Silicon Defects	0.3ev	1.07
Electromigration	1.0ev	1.26
Ion Contamination	1.4ev	1.39

Table 1: Reliability Degradation for Memory Chip

5. Complex Activity Experiment

The effect of different types of activity was investigated by observing the thermal activity in an Intel 7848 Microcontroller. The microcontroller incorporates an ALU, RAM and ROM on a single die and is shown in block diagram form in figure 3. The inclusion of these functional units on a single die provided the opportunity to view the effects of concurrent and complex activity.

A repeated NOP operation was used to establish the base level. An ALU intense operation which involved indirect addressing of the on-board RAM (refer to figure 3) was used to observe the

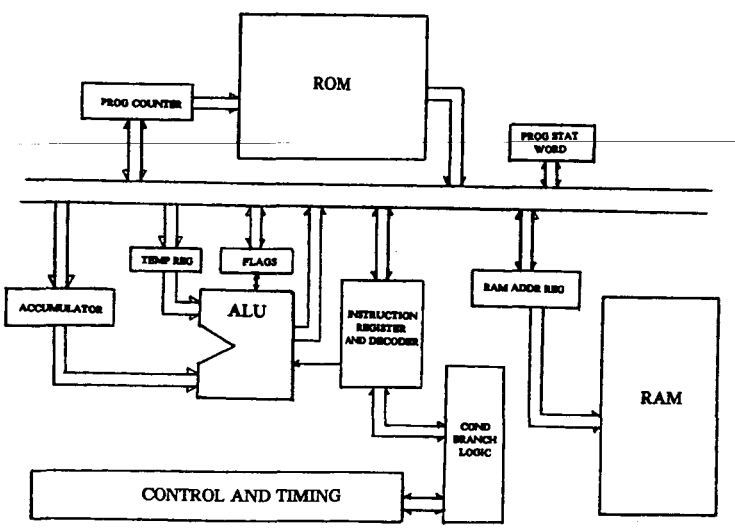

Figure 3: Block Diagram of Micro-controller

effects of a complex activity. The operation involved use of the ALU and an indirect accesses to the RAM in addition the base level activity of instruction fetch and decoding.

The results of the experiment are shown in figure 4. Acceleration factors corresponding to thermal activation energies in the range 0.3 to 1.4ev were computed by equation 2 (see table 2). Here again the impact of change in activity on reliability degradation is evident. The difference between a NOP and complex activity is seen to lower the system reliability by as much as 55 percent. Here it would seem from the results that both frequency of access and complexity of the access have a strong effect on the reliability of computer logic.

Processor Activity		
Failure Mechanism	Activation Energy	Acceleration Factor
Silicon Defects	0.3ev	1.10
Electromigration	1.0ev	1.36
Ion Contamination	1.4ev	1.55

Table 2: Reliability Degradation for Micro-controller

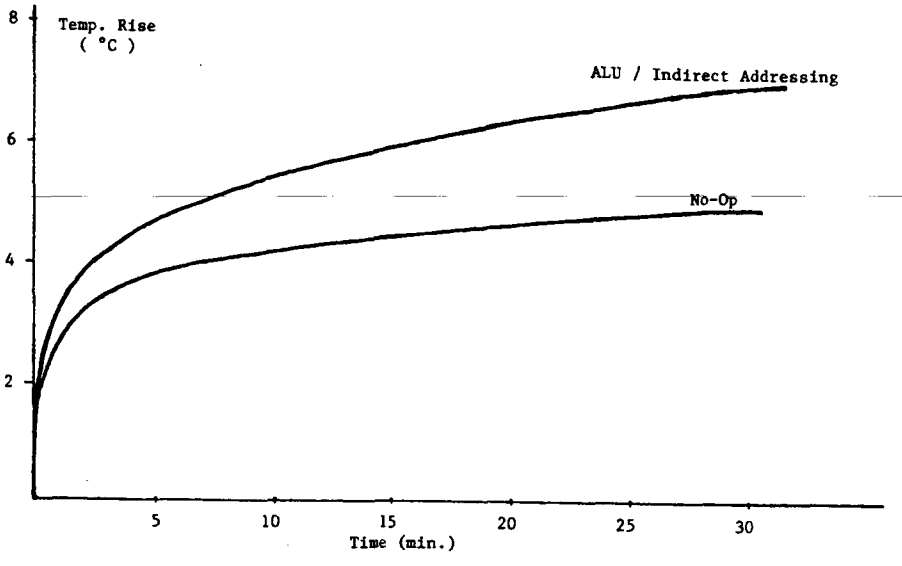

Figure 4: Access Complexity Results

6. Concluding Remarks

The preliminary experimental results gathered in this investigation indicate that variations in concurrent activity can result in thermal degradation of more than 50 percent for some failure mechanisms. The impact of this result on large systems with external cooling facilities is yet to be determined. With decreasing device dimensions and increasing concurrent chip activity, however, this source of thermal degradation is likely to increase in importance. More measurement-based research in VLSI chip reliability is needed to determine the full impact of activity related failure modes and to incorporate the measured effects into accurate reliability models.

7. Acknowledgement

The authors thank Prof. Ricardo Uribe for the use of the Advanced Digital Systems Laboratory and the UIUC Infrared Interest Group, especially Prof. James Heath, for the use of the thermograph. This work was supported in part by NASA grant NAG-1-602 and in part by the Semiconductor Research Corporation (SRC) under contract RSCH 84-06-049.

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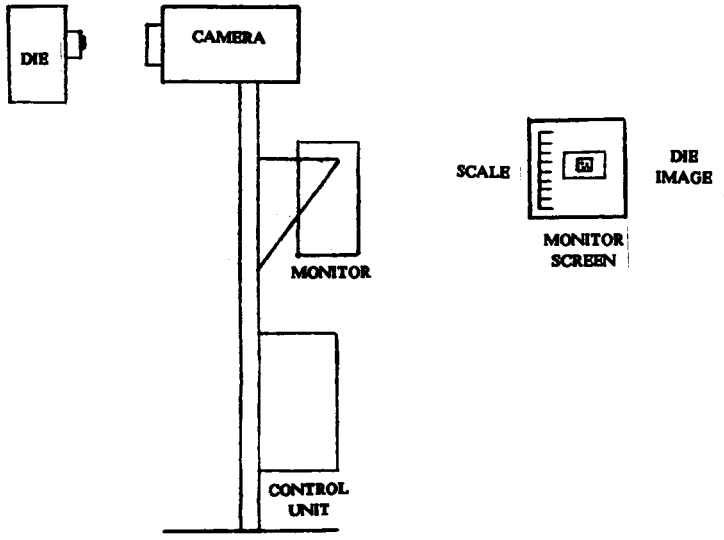
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CAMERA
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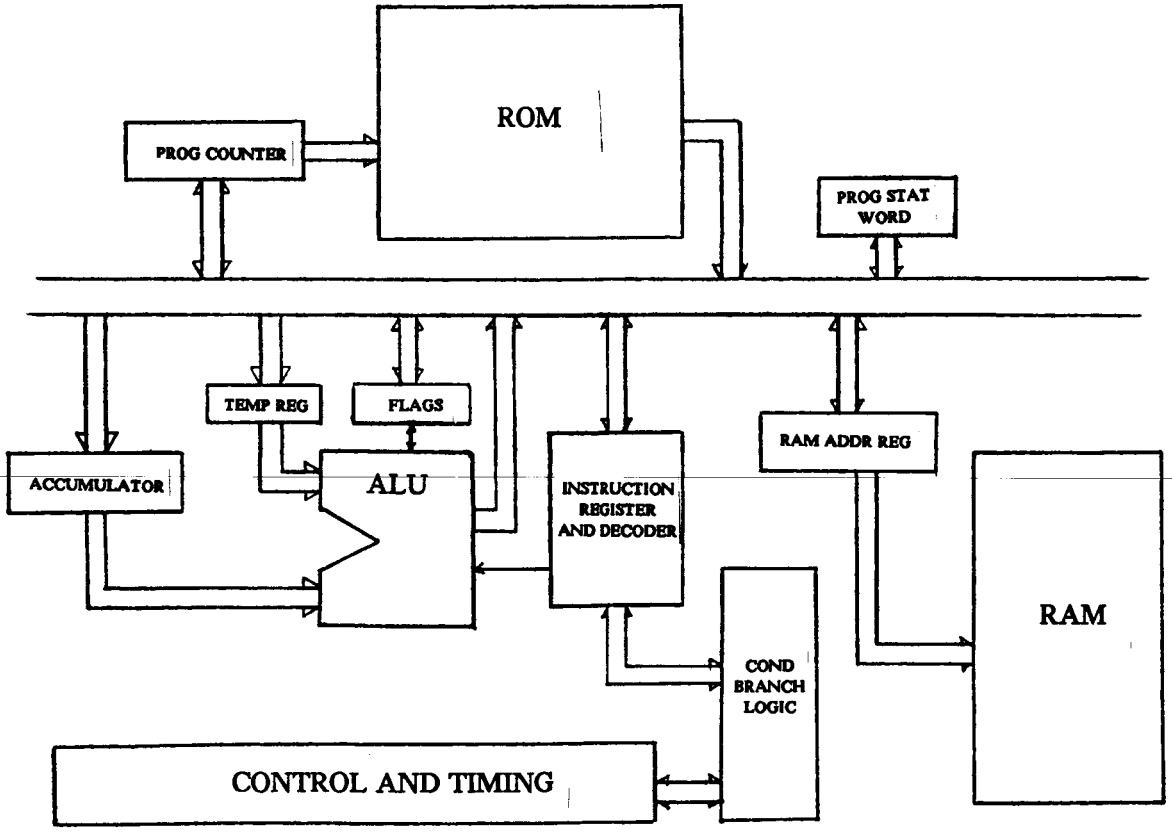
ROM
PROG COUNTER
PROG STAT WORD
TEMP REG
FLAGS
ACCUMULATOR
ALU
INSTRUCTION REGISTER AND DECODER
RAM ADDR REG
RAM
COND BRANCH LOGIC
CONTROL AND TIMING